```
;PALASM Design Description

;------------------------- Declaration Segment ---------------------

TITLE     INTER12 - Interrupt Controller for 68000
PATTERN   U29 of Control Board
REVISION  1.2
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COMPANY   ELECTROHOME LTD.
DATE      01/26/93

CHIP  INTER  PALCE610

;------------------------- Description ----------------------------
;
; This IC captures interrupts and inputs them to the 68000. There
; are five interrupt sources:
;
;          Interrupt  Level  IPL Code  Priority
;
;            VDRIVE     7      000     highest
;            DPB        6      001       -
;            IOP        5      010       -
;            ACON       4      011       -
;            TIMER      3      100     lowest
;
; The VDRIVE interrupt occurs on the leading edge of the active-high
; VDRIVE (V-DRIVE) signal from the DPB. It is normally non-maskable,
; but becomes disabled when NO_NMI (NO-NMI) from U16 (68HC711D3
; microcontroller) is driven high. The DPB, IOP and ACON interrupts
; indicate a read from or write to the 68000 by the DPB, IOP (U16)
; or ACON hardware, respectively. TIMER interrupts are generated at
; 10 msec intervals by U16 for use by the 68000 software.
;
; U29 individually and asynchronously captures interrupts from all
; five sources (on low-to-high transitions) and encodes them with a
; priority encoder, creating IPL2, IPL1 and IPL0 (the IPL code)
; which are input to the 68000. On receipt of a code other than 111,
; the 68000 begins an interrupt cycle. An interrupt acknowledge
; signal (IACK*) is then created by U28 and input to the 68000 on its
; VPA* pin. This allows an "autovector" to occur. U29 stores the
; interrupts and presents them in priority order to the 68000. The
; 68000 software is responsible for clearing captured interrupts
; immediately after responding to them by writing to an "interrupt
; capture" register in U29. This will strobe the active low register
; select input CS_INT (CS-INT*).
;
;
; Revision History:
;
;   V1.0 - original
;
;   V1.1 - Modified priority encoder to block VDRIVE code (000) when
;          NO_NMI is high, eliminating the possiblility of a noise
;          pulse creating a non-maskable interrupt during power-up.
;
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